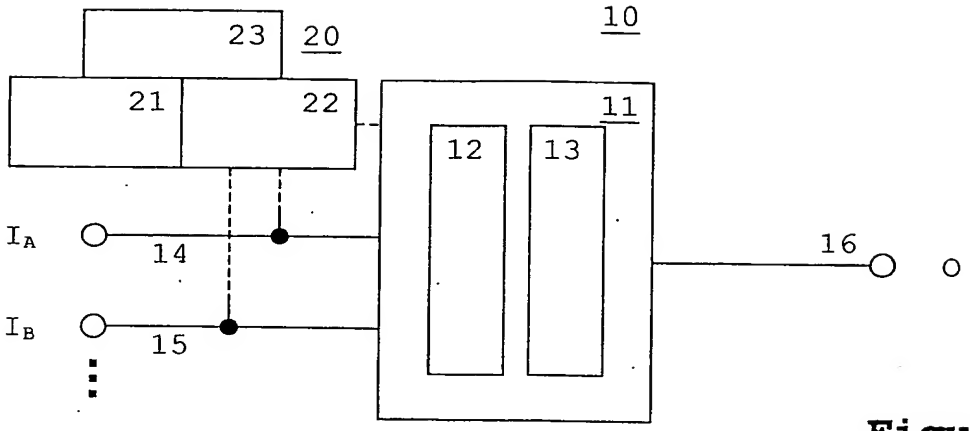
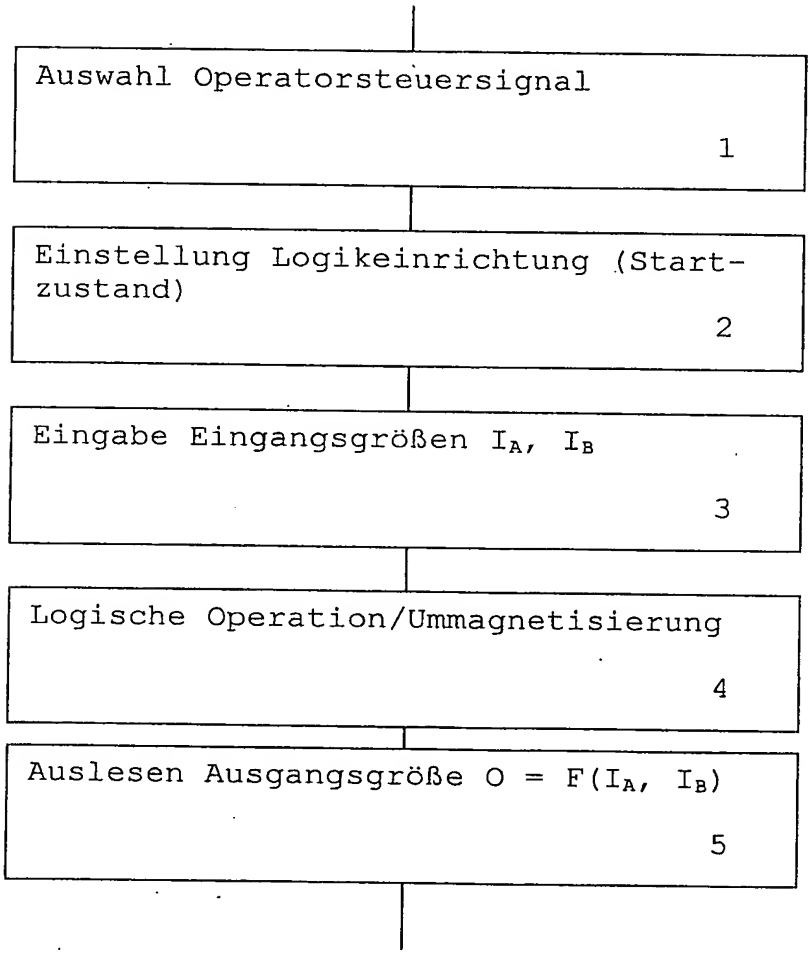
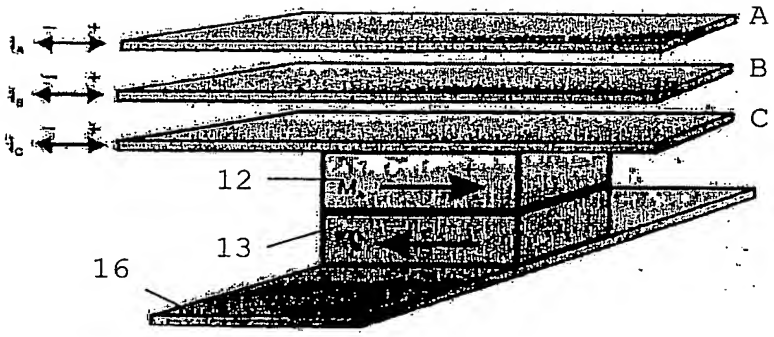


Figur 1



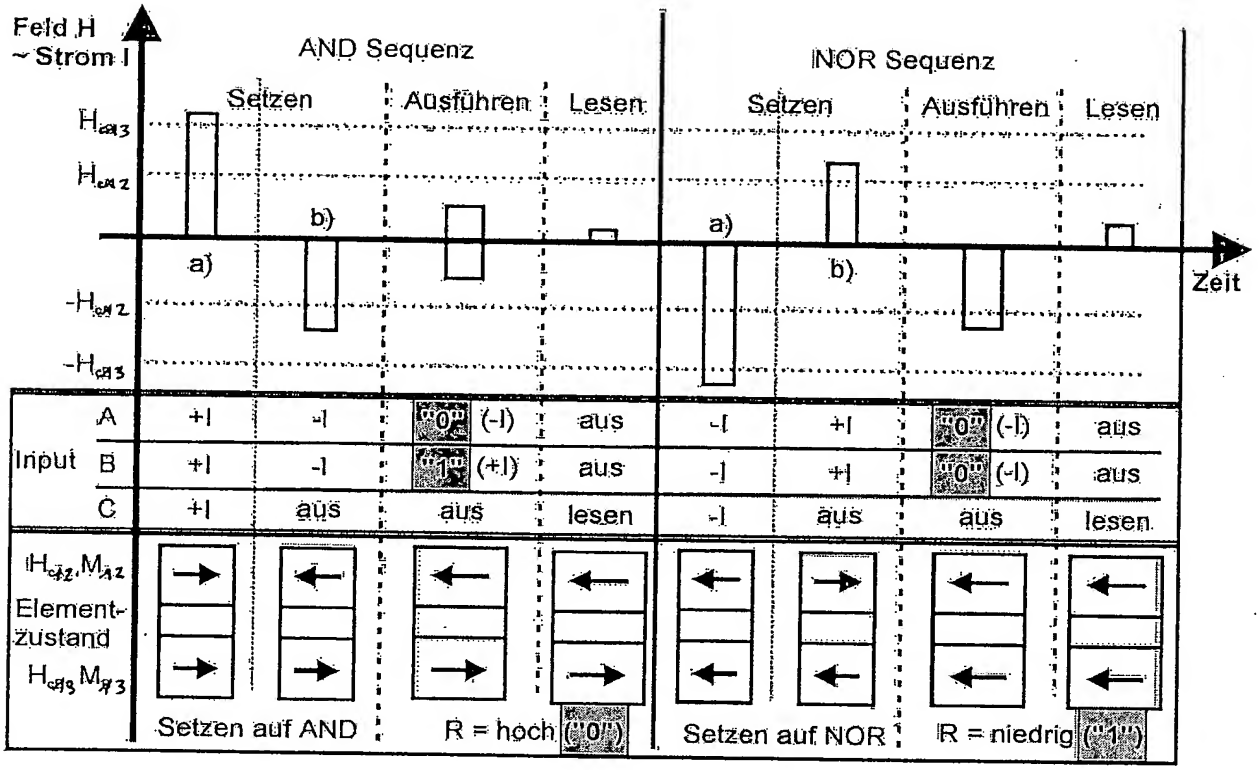
Figur 2



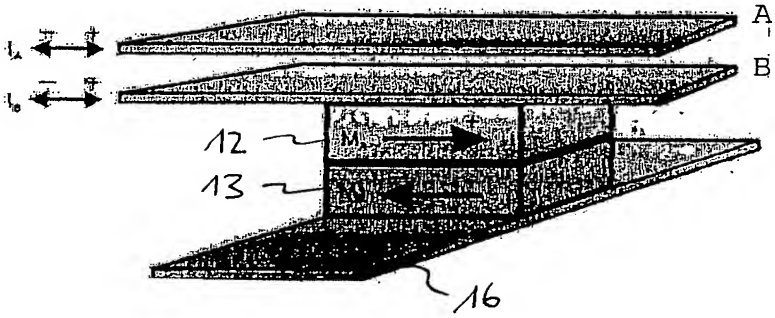
Figur 3

SET-Sequenz für Ausgangszustand	input A -I (0) input B -I (0)	input A -I (0) input B +I (1)	input A +I (1) input B -I (0)	input A +I (1) input B +I (1)	Logiktabelle	
A,B,C=+I A,B=+I	R = high (0)	R = low (1)	R = low (1)	R = low (1)	A B out 0 0 0 1 0 1 0 1 1 1 1 1	OR
A,B,C=+I A,B=-I	R = high (0)	R = high (0)	R = high (0)	R = low (1)	A B out 0 0 0 1 0 0 0 1 0 1 1 1	AND
A,B,C=-I A,B=+I	R = low (1)	R = high (0)	R = high (0)	R = high (0)	A B out 0 0 1 1 0 0 0 1 0 1 1 0	NOR
A,B,C=-I A,B=-I	R = low (1)	R = low (1)	R = low (1)	R = high (0)	A B out 0 0 1 1 0 1 0 1 1 1 1 0	NAND

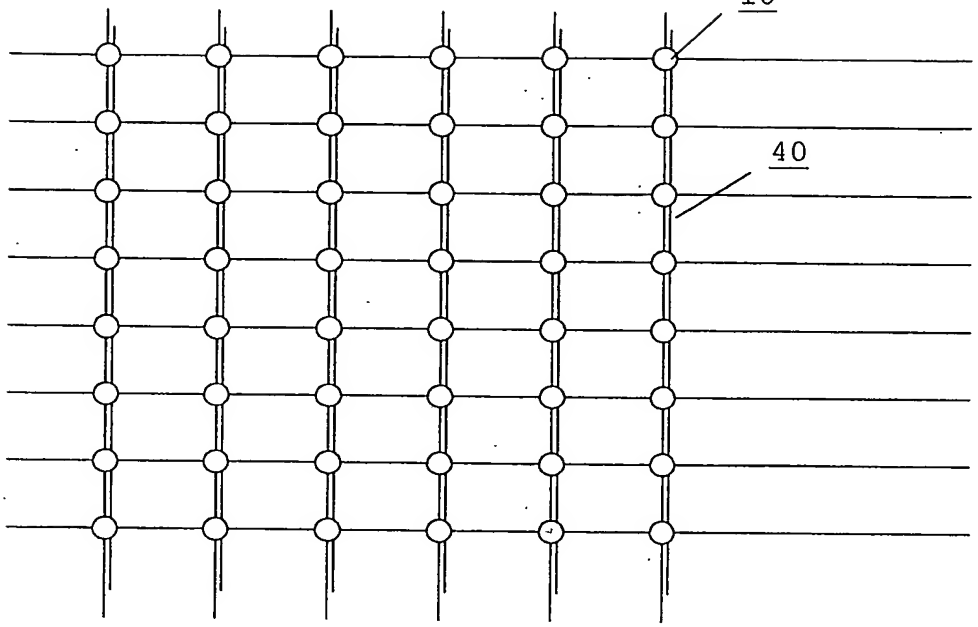
Figur 4



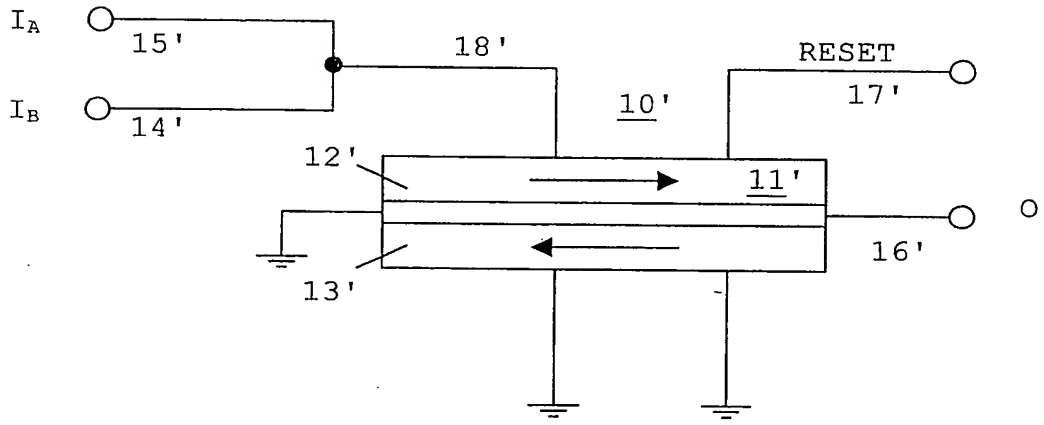
Figur 5



Figur 6



Figur 7



Figur 8 (Stand der Technik)